A RIGOROUS STUDY OF WIRE-BONDING AND VIA-HOLE EFFECTS ON GaAs FIELD EFFECT TRANSISTORS†

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Abstract

A new procedure is presented for evaluation of the wire-bonding and via-hole effects on a GaAs FET at microwave frequencies. The analysis not only provides a rigorous characterization of the passive elements, like bond-wires, via-holes and microstrips, on a GaAs FET but also includes their mutual coupling with the active region. For practical applications, the corresponding gate, source and drain inductances, which are the important extrinsic parameters of a CAD oriented equivalent circuit model, are extracted based on the calculated S parameters.

I. Introduction

It is a well known property that the variations of the gain and noise figure parameters of a GaAs FET due to bond-wires and via-holes become more evident at higher microwave frequencies. Provision of accurate characterization data representing the effects of such elements is therefore of primary importance for every GaAs FET manufacturer. Generally speaking, the most commonly used small-signal equivalent circuit model for a GaAs FET can be divided into two parts: the intrinsic parameters and the extrinsic parameters. The intrinsic parameters characterize the active region and are functions of biasing conditions, whereas the extrinsic parameters result from the passive elements and depend on the geometrical parameters of bond-wires, via-holes, microstrips, substrates etc.

Numerous approaches for direct extraction of the intrinsic and extrinsic parameters from measured S-parameter data has been discussed since years [1]-[3]. To achieve the best results for extrinsic parameters, the FET should be measured in the medium in which it will be used. However, the actual measurement of the S parameters is made in a test fixture using a network analyzer. The style of the fixture will greatly influence the measurement. Recently, the full-wave numerical techniques make rapid progress in analyzing the three-dimensional metallization structures in a layered medium. Accurate investigation of bond-wires and via-holes connected to microstrip lines has been demonstrated. [4],[5] It is observed that these passive elements were studied in an isolated situation. The application to FET models is of limited value since it does not account for the mutual coupling among the passive elements as well as the active region of a FET.

In this analysis, the metallization parts of a FET are replaced by current density distribution, whereas the active region is represented by a widely used 10-element equivalent circuit model. To satisfy the boundary conditions on the metallization structure and the I-V characteristics of the active region obtained from the equivalent circuit model, an electric-field integral equation can be derived. An iterative method of moments is then developed to solve the integral equation and find the current distribution on microstrip lines, and subsequently the S parameters and the equivalent gate, source and drain inductances.

II. Theory

1. The Equivalent Circuit of the Active Region

Fig. 1 shows a typical common source configuration for a GaAs FET. For this structure to function as an amplifier, proper bias conditions needs to be established. This determines the values of intrinsic parameters of a small-signal equivalent circuit as illustrated in Fig. 2(a). To derive the electric-field integral equation associated with the FET conveniently, the circuit is simplified as that in Fig. 2(b) in which the expressions of circuit elements are given as

$$Z_g(\omega) = R_g + \frac{1}{j\omega C_{gs}} + R_i - \frac{T_g(\omega)}{T_n(\omega)}, \quad (1)$$

$$Z_d(\omega) = R_d + Z_{ds}(\omega) - \frac{T_d(\omega)}{T_n(\omega)}, \quad (2)$$

$$Z_s(\omega) = R_s + \frac{T_s(\omega)}{T_n(\omega)}, \quad (3)$$

$$V_e(I_g, \omega) = I_g \frac{T_e(\omega)}{T_n(\omega)} \quad (4)$$

where

$$T_g(\omega) = (R_i^2 + R_i Z_{ds}(\omega))(\frac{1}{C_{gd}} + \frac{1}{C_{dc}} + \frac{1}{C_{gs}}) + \frac{G(\omega)Z_{ds}(\omega)R_i}{j\omega C_{gs}C_{gd}} + \frac{R_i + Z_{ds}(\omega)}{j\omega C_{gs}^2} + \frac{1}{j\omega C_{gs}C_{dc}}(2R_i + Z_{ds}(\omega) + G(\omega)Z_{ds}(\omega)R_i + \frac{1 + G(\omega)Z_{ds}(\omega)}{j\omega C_{gs}}), \quad (5)$$

$$T_d(\omega) = (\frac{1}{C_{gd}} + \frac{1}{C_{dc}} + \frac{1}{C_{gs}})(Z_{ds}^2(\omega) + Z_{ds}(\omega)R_i) + \frac{Z_{ds}(\omega) + G(\omega)Z_{ds}^2(\omega)}{j\omega C_{dc}C_{gs}}, \quad (6)$$

$$T_s(\omega) = Z_{ds}(\omega)R_i(\frac{1}{C_{gd}} + \frac{1}{C_{dc}} + \frac{1}{C_{gs}}) + \frac{Z_{ds}(\omega)}{j\omega C_{dc}C_{gs}}, \quad (7)$$

$$T_n(\omega) = (\frac{1}{C_{gd}} + \frac{1}{C_{dc}} + \frac{1}{C_{gs}})(R_i + Z_{ds}(\omega)) + \frac{1}{C_{dc}}(\frac{1 + G(\omega)Z_{ds}(\omega)}{j\omega C_{gs}} + \frac{1}{j\omega C_{gd}}), \quad (8)$$

$$T_e(\omega) = \frac{G(\omega)Z_{ds}(\omega)}{\omega^2 C_{gs}C_{dc}C_{gd}} - \frac{G(\omega)Z_{ds}(\omega)R_i}{j\omega C_{gs}C_{gd}}, \quad (9)$$

$$Z_{ds}(\omega) = \frac{R_{ds}}{1 + j\omega R_{ds}C_{ds}}, \quad (10)$$

$$G(\omega) = g_m e^{-j\omega\tau} \quad (11)$$

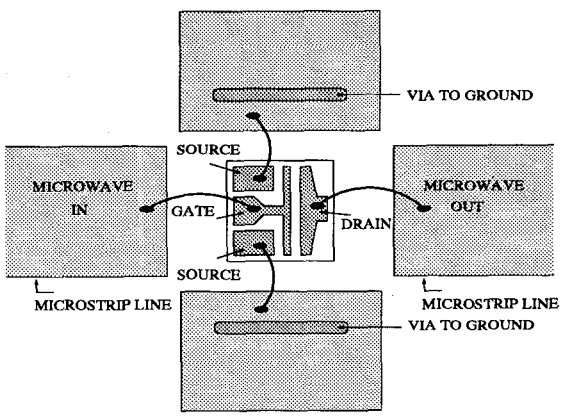

Figure 1: The common source configuration of a GaAs FET.

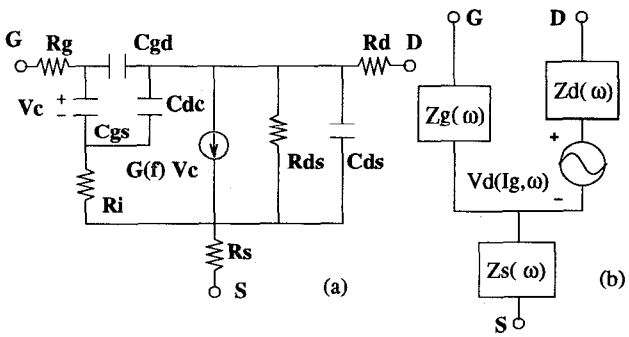

Figure 2: (a) The small-signal equivalent circuit of a GaAs FET. (b) A simplified circuit of (a).

2. Full-Wave Analysis of the Passive Elements

The currents over all the conductors of a FET can be treated as a continuous distribution of Hertzian dipoles. In the Green's function formulation the electric field is written as

$$\vec{E}(x,y,z) = \int_{\text{metal}} \overline{\overline{G}}(x-x', y-y', z-z') \cdot \vec{J}(x', y', z') dx' dy' dz' \quad (12)$$

where $\overline{\overline{G}}$ is the dyadic Green's function with respect to the GaAs substrate structure and $\vec{J}$ is the volume current density distributed on the metallization structure. If the perfect conductor is assumed, an electric-field integral equation can be obtained by imposing the boundary condition that the total electric field inside the conductor is zero:

$$\vec{E}(x,y,z) + \vec{E}_{inc}(x,y,z) + \vec{E}_{act}(x,y,z) = 0, \quad \text{for } x,y,z \text{ inside the conductor.} \quad (13)$$

It is noted that E_{inc} and E_{act} represent an impressed electric field generated at the input end and at the active region, respectively. The method of moments is used to transform (13) into a matrix equation. For simplicity, the bond-wires, via-holes and microstrips of a FET are restricted to a rectangular shape, as shown in Fig. 3. Expanded by pulse and roof-top basis functions, the volume current density is formulated as

$$\begin{aligned}
\vec{J}(x',y',z') &= \hat{x}\sum_m \frac{I_x^m}{d_y} t(\frac{x'-x_m}{d_x}) p(\frac{y'-y_m}{d_y}) \delta(z'-h) \\
&+ \hat{x}\sum_{m'} \frac{I_x^{m'}}{d_y} t(\frac{x'-x_{m'}}{d_x}) p(\frac{y'-y_{m'}}{d_y}) \delta(z'-h-b) \\
&+ \hat{y}\sum_n \frac{I_y^n}{d_x} p(\frac{x'-x_n}{d_x}) t(\frac{y'-y_n}{d_y}) \delta(z'-h) \\
&+ \hat{y}\sum_{n'} \frac{I_y^{n'}}{d_x} p(\frac{x'-x_{n'}}{d_x}) t(\frac{y'-y_{n'}}{d_y}) \delta(z'-h-b) \\
&+ \hat{z}\sum_l \frac{I_z^l}{d_x d_y} p(\frac{x'-x_l}{d_x}) p(\frac{y'-y_l}{d_y}) p(\frac{z'-z_l}{h}) \\
&+ \hat{z}\sum_{l'} \frac{I_z^{l'}}{d_x d_y} p(\frac{x'-x_{l'}}{d_x}) p(\frac{y'-y_{l'}}{d_y}) p(\frac{z'-z_{l'}}{b}) \\
&+ \hat{z}\frac{I_{inc}}{d_x d_y} p(\frac{x'-x_i}{d_x}) p(\frac{y'-y_i}{d_y}) p(\frac{z'-z_i}{h}) \\
&+ \hat{z}\frac{I_g}{d_x d_y} p(\frac{x'-x_g}{d_x}) p(\frac{y'-y_g}{d_y}) p(\frac{z'-z_g}{d}) \\
&+ \hat{z}\frac{I_s}{d_x d_y} p(\frac{x'-x_s}{d_x}) p(\frac{y'-y_s}{d_y}) p(\frac{z'-z_s}{d}) \\
&+ \hat{z}\frac{I_d}{d_x d_y} p(\frac{x'-x_d}{d_x}) p(\frac{y'-y_d}{d_y}) p(\frac{z'-z_d}{d})
\end{aligned} \quad (14)$$

where

$$t(u) = \begin{cases} 1-|u|, & |u| \le 1 \\ 0, & |u| > 1, \end{cases} \quad (15)$$

and

$$p(u) = \begin{cases} 1, & |u| \le \frac{1}{2} \\ 0, & |u| > \frac{1}{2}. \end{cases} \quad (16)$$

Note that I_{inc} is the incident current excited by a sinusoidal voltage V_{inc}, placed at the input end. I_g, I_d and I_s represent the current on the gate, source and drain respectively. They have to satisfy the relation:

$$I_g + I_d + I_s = 0. \tag{17}$$

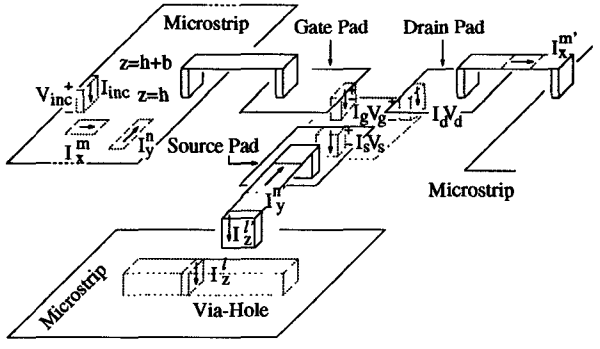

Figure 3: Three-dimensional modeling of a GaAs FET.

3. The Matrix Formulation

As suggested in Fig. 3, equation (17) is approximately correct for connecting all the bond-wires to an imaginary patch of sufficiently small size. In the meantime, the patch is assumed to be equipotential such that the voltage drops inside the active region can be approximated as

$$V_g = I_g Z_g(\omega), \tag{18}$$
$$V_s = I_s Z_s(\omega), \tag{19}$$
$$V_d = I_d Z_d(\omega) + V_e(I_g, \omega). \tag{20}$$

With the testing functions chosen to be the same as the expansion functions, the moment method procedure results in a matrix equation in the form

$$\begin{bmatrix} [Z_{I_x I_x}] & [Z_{I_x I_y}] & [Z_{I_x I_z}] \\ [Z_{I_y I_x}] & [Z_{I_y I_y}] & [Z_{I_y I_z}] \\ [Z_{I_z I_x}] & [Z_{I_z I_y}] & [Z_{I_z I_z}] \end{bmatrix} \begin{bmatrix} [I_x] \\ [I_y] \\ \begin{bmatrix} I_z^1 \\ \bullet \\ \bullet \\ \bullet \\ I_{inc} \\ \bullet \\ \bullet \\ \bullet \\ \bullet \\ I_g \\ I_s \\ I_d \end{bmatrix} \end{bmatrix} = \begin{bmatrix} [0] \\ [0] \\ \begin{bmatrix} 0 \\ \bullet \\ \bullet \\ 0 \\ V_{inc} \\ 0 \\ \bullet \\ \bullet \\ 0 \\ V_g \\ V_s \\ V_d \end{bmatrix} \end{bmatrix}. \tag{21}$$

The computation of each reaction element $Z_{I_u I_v}$ in the left-hand side matrix can be performed using a spectral-domain approach [6]. Substituting (18) ~ (20) into (21), one will find that the right-hand side column matrix contains the unknown current coefficients which are not removable. Under this situation, an iterative scheme will be required to solve for the coefficients [7]. The S parameters are further extracted from knowledge of the current distribution and the propagation constant of the dominant microstripline mode.

III. Numerical Results

1. The Common Source Configuration

Fig. 4(a) shows the layout of a common source configuration. With the calculated results of the S parameters, one can approximate the values of the equivalent gate, source and drain inductances using the following expressions:

$$L_g \simeq \frac{Z_0}{j\omega} \frac{(1+S_{11})(1-S_{22}) + S_{12}S_{21} - 2S_{12}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}} - \frac{Z_g(\omega)}{j\omega}, \tag{22}$$
$$L_s \simeq \frac{Z_0}{j\omega} \frac{2S_{12}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}} - \frac{Z_s(\omega)}{j\omega}, \tag{23}$$
$$L_d \simeq \frac{Z_0}{j\omega} \frac{(1-S_{11})(1+S_{22}) + S_{12}S_{21} - 2S_{12}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}} - \frac{Z_d(\omega)}{j\omega} \tag{24}$$

where Z_0 is the characteristic impedance of the microstrip line. The results of equivalent inductances are shown in Fig. 4(b). For a self-consistency check, the S parameters are compared with those calculated from the equivalent circuit model, as plotted in Fig. 5. Good agreement is observed over a wide frequency range.

2. The Common Gate Configuration

Fig. 6(a) shows the layout of a common gate configuration. The corresponding equivalent inductances can be approximated as

$$L_g \simeq \frac{Z_0}{j\omega} \frac{2S_{12}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}} - \frac{Z_g(\omega)}{j\omega}, \tag{25}$$
$$L_s \simeq \frac{Z_0}{j\omega} \frac{(1+S_{11})(1-S_{22}) + S_{12}S_{21} - 2S_{12}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}} - \frac{Z_s(\omega)}{j\omega}, \tag{26}$$
$$L_d \simeq \frac{Z_0}{j\omega} \frac{(1-S_{11})(1+S_{22}) + S_{12}S_{21} - 2S_{12}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}} - \frac{Z_d(\omega)}{j\omega}. \tag{27}$$

In a similar fashion we plot the results of the inductances and the S parameters in Fig. 6(b) and Fig. 7, respectively.

IV. Conclusion

A theoretical approach for studying the wire-bonding and via-hole effects on a GaAs FET was given. Through the arrangement of the bond-wire and via-hole locations, the FET has been connected in common source or common gate configuration. The corresponding scattering parameters and the equivalent gate, source and drain inductances were extracted from a full-wave solution of the current distribution on microstrip lines.

References

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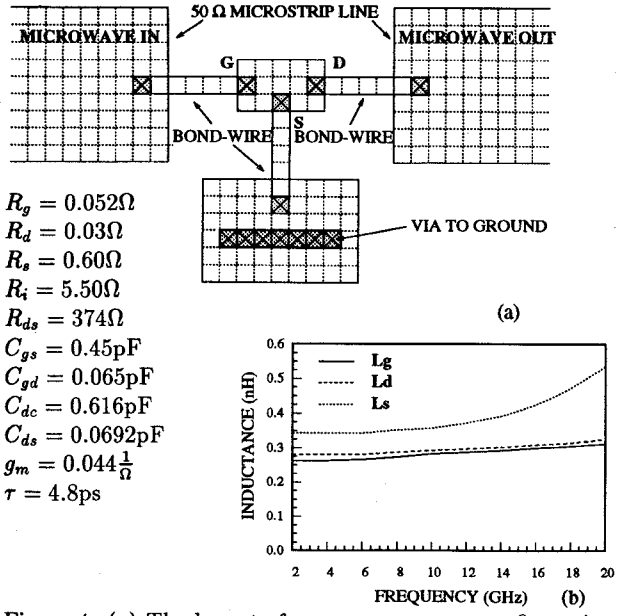

Figure 4: (a) The layout of a common source configuration. (b) The equivalent gate, source and drain inductances versus frequency.

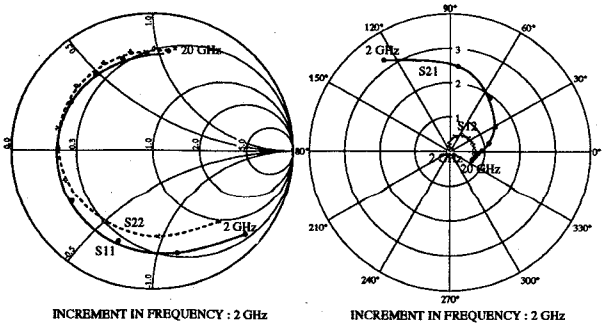

Figure 5: The comparison of the scattering parameters extracted from the current distribution on the microstrip lines (solid and dashed curves) and calculated from the equivalent circuit model (dark and gray circules) for a common source configuration.

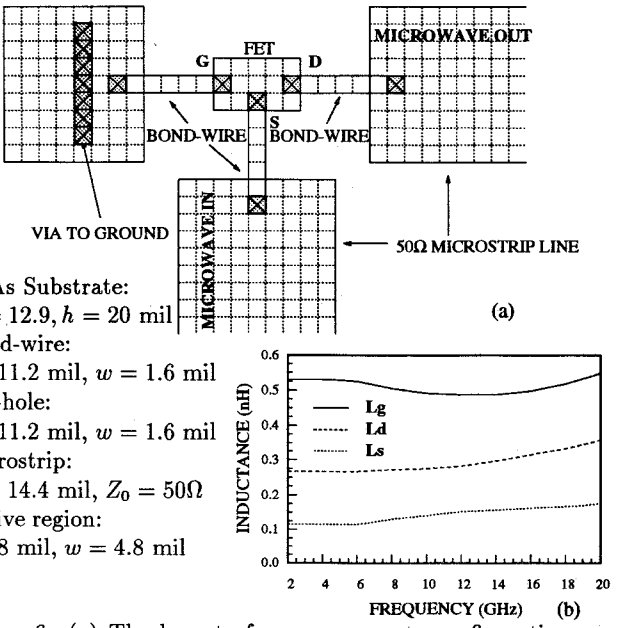

Figure 6: (a) The layout of a common gate configuration. (b) The equivalent gate, source and drain inductances versus frequency.

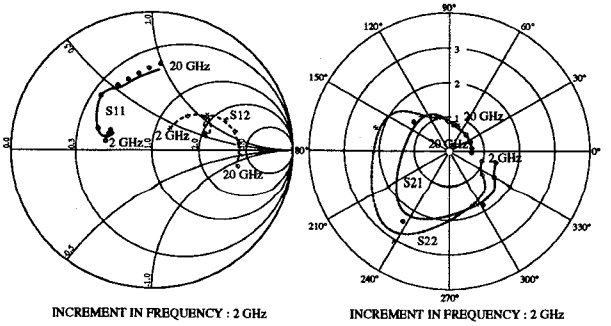

Figure 7: The comparison of the scattering parameters extracted from the current distribution on the microstrip lines (solid and dashed curves) and calculated from the equivalent circuit model (dark and gray circules) for a common gate configuration.